



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/686,794

10/16/2003

Chia-Ta Hsieh

TS01-280B

9636

24504

7590

11/03/2004

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
100 GALLERIA PARKWAY, NW
STE 1750
ATLANTA, GA 30339-5948

EXAMINER

WILSON, SCOTT R

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/686,794

Applicant(s)

HSIEH, CHIA-TA

Examiner

Scott R. Wilson

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 and 25-31 is/are pending in the application.
- 4a) Of the above claim(s) 25-31 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>1/15/04</u> . | 6) <input type="checkbox"/> Other: _____ |

Art Unit: 2826

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-13 in the response filed 23 September 2004 is acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 recites the limitation "and TG" in the second line of the claim. There is insufficient antecedent basis for this limitation in the claim. There is no antecedent basis for a transfer gate in the dependency from claims 3 or 4.

Claim 12 recites the limitation "said first floating gate transistor" in the second line of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Art Unit: 2826

Claims 1-4, 6, 7 and 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Ma et al.. As to claim 1, Ma et al., Figure 2A, discloses a multi-bit split-gate (MSG) flash cell comprising: a semiconductor substrate (26) having a surface region; a first drain region (22A) and a second drain region (20A) formed in said surface region, a plurality of $(N + 1)$ stacked gates (20) and (22), where N is equal to one, separated apart by N select gates (SGs) (24) between said first drain region and said second drain region, a first bit line contacting said first drain region (Figure 2B, element 22A), a second bit line contacting said second drain region (Figure 2B, element 20A), and a word line (Figure 2B, element 28) contacting said select gate.

As to claim 2, Ma et al., Figure 2A, discloses that said surface region is of first conductivity type, embodied as p-type.

As to claim 3, Ma et al., Figure 2A, discloses that said first and second drain regions are of second conductivity type, embodied as n-type, which is opposite the conductivity type of the surface region.

As to claim 4, Ma et al., Figure 2A, discloses that the stacked gates (20) and (22) comprise a floating gate (22B) and (20B) and a control gate (22C) and (20C).

Claim 5 is rejected under 35 U.S.C. 102(a) as being anticipated by applicants prior art. Applicant discloses, in Figure 1b, which is a schematic representation of Ma et al., and page 5, line 16, that the control gate and transfer gate are structurally identical, which is within the scope of the transfer/control gate being addressable as a transfer gate with one address and as a control gate with a different address.

As to claim 6, Ma et al., Figure 2A, discloses that the floating gate (20B) comprises a first polysilicon layer (Abstract) separated from said surface region by a first dielectric layer (20D)

As to claim 7, Ma et al., Figure 2A, discloses that the control gate (20C) comprises a second polysilicon layer (Abstract) separated from the first polysilicon layer by a second dielectric layer (20E).

As to claim 11, Ma et al., Figure 2A, discloses that the select gate (24A) is shared by adjacent stacked gates (22) and (20).

Art Unit: 2826

As to claim 12, Ma et al., Figure 2A, discloses that the adjacent floating gate transistors (20) and (22) and the select gate (24) must all be active to turn on the memory cell.

As to claim 13, Ma et al., Figure 2B, discloses that the word line (28) is oriented to be normal to said first bit line (22A) and said second bit line (20A).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma et al. in view of Yuan et al.. As to claim 8, Ma et al., Figure 2A, discloses the device of claim 1, as described above. Ma et al. does not disclose expressly the first and second bit lines formed from polysilicon. Yuan et al. discloses (col. 6, lines 51-52) bit lines formed from polysilicon in a non volatile memory cell array. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the polysilicon bit lines of Yuan et al. in the device of Ma et al. The motivation for doing so would have been to reduce the bit line resistance relative to a bit line formed, for example, as a diffusion. Therefore, it would have been obvious to combine Yuan et al. with Ma et al. to obtain the invention as specified in claim 8.

As to claim 9, Ma et al., Figure 2A, discloses the device of claim 1, as described above. Ma et al. does not disclose expressly the first and second word lines formed from polysilicon. Yuan et al. discloses (col. 7, lines 35-36) word lines formed from polysilicon in a non volatile memory cell array. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the polysilicon word lines of Yuan et al. in the device of Ma et al. The motivation for doing so would have been to reduce the word line resistance relative to a word line formed, for example, as a diffusion. Therefore, it would have been obvious to combine Yuan et al. with Ma et al. to obtain the invention as specified in claim 8.

Art Unit: 2826

As to claim 10, Yuan et al., Figure 3, discloses that the word lines (91), (92), (93) and (94) are separated from the bit lines (81), (82), (83), (84) and (85) by a dielectric layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

srw
October 29, 2004